Electronic Version
Stylesheet Version v1.1.1

DYNAMIC RANDOM ACCESS MEMORY WITH SMART REFRESH SCHEDULER

Abstract

In a DRAM, which includes a plurality of memory banks, there is a pair of separate flag bit registers for each bank with the flag bit registers that are shifted up/down respectively. A comparator for each bank provides a comparator output. An arbiter for each bank is connected to receive a flag bit up signal and a flag bit down signal from the flag bit registers for that bank and the comparator output from the comparator for that bank. The arbiters are connected to receive a conflict in signal and to provide a conflict out signal. The pair of flag bit registers represent a refresh status of each bank and designate memory banks or arrays that are ready for a refresh operation.